System MMU

Reference : RTL

System MMU provides 2 main functions :

- Virtual to physical address translation
- Memory protection

System MMU upstream port can be directly connected to 1 master and used as a dedicated MMU or connected to multiple masters via an interconnect and so used as a shared MMU.

It allows non-CPU master to see contiguous memory space and remove the need to allocate fixed physical memory space or to manage memory fragmentation via a scatter-gather DMA.

Memory translation, attributes and validity information are contained in a set of translation tables located in downstream memory.

System MMU supports secure and non-secure context but doesn't support virtualization.

HDL: Verilog.

Verification Language: Python

CAD Tools (Open tools):

- Simulation tool: Icarus Verilog
- TestBench environment: Cocotb
- Code Coverage tool: Covered
- Synthesis suite: Yosys

System MMU – Functional Specification

System MMU – Test Bench Description

System MMU – Delivery Description

System MMU home directory