Choosing the Best Processor for Your Audio DSP Application

Paul Beckmann

DSP Concepts

AUDIO AES 137TH AES CONVENTION

About Paul Beckmann

1984-1992. M.I.T. Received SB, SM, and PhD in EE specializing in DSP under Prof. Bruce Musicus.

1992-2001. Bose Corporation

2001-2003 Enuvis Corporation

2003- DSP Concepts

Founder and CTO

Providing tools and design services to audio product developers

Key skills

DSP algorithms and optimization

Audio product design

Passionate about audio design tools

Outline

- Problem statement
- Comparing processor architectures
- DSP benchmarks
- Benchmarking with Audio Weaver
- Conclusion

The Audio Product Development Challenge

- Complexity of audio products is increasing
- Development times are shrinking
- Multiple audio formats
- Connectivity
- Software updates
- Have to integrate 3rd party IP
- Size and power requirements

Multiple Skill Sets Required

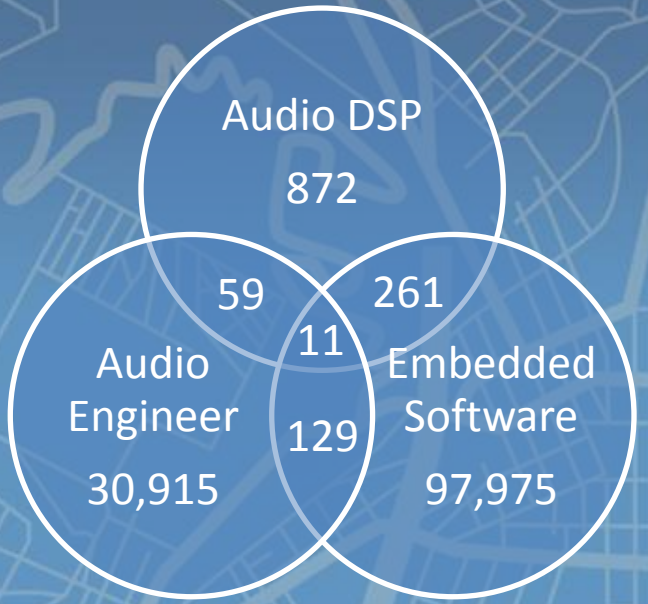
Electrical

Mechanical

Acoustical

User interface

Audio processing software requires multiple skills

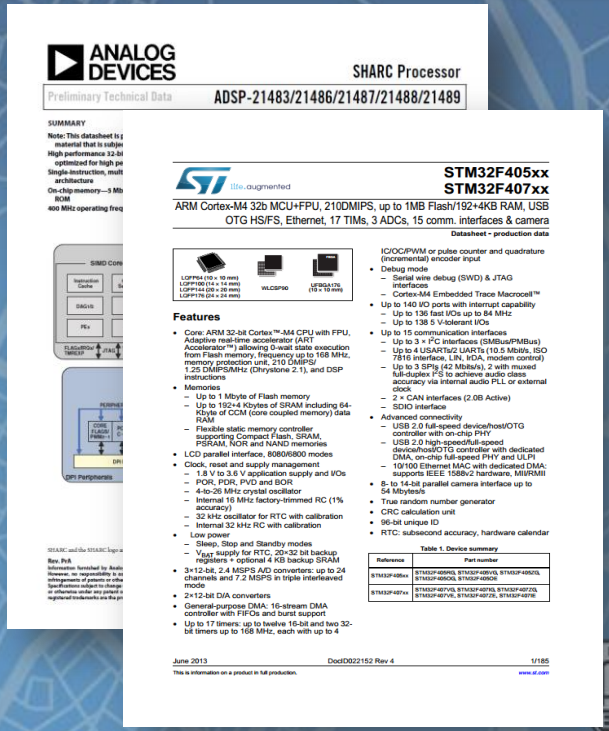


More Processor Choices

- Analog Devices
  - *SHARC, Blackfin, SigmaDSP*
- Texas Instruments
  - *C55, C67x, C66x*
- ARM
  - *ARM 9 / 11*
  - *Cortex-M4 / M7*
  - *Cortex-A8 / A9 / A15 / etc.*
- Intel x86 / x64
- And embedded cores
  - *Tensilica, CEVA, and ARC*

System Design Issues

- Peripherals
  - *Serial ports*
  - *Connectivity*
  - *Sample rate converters*
  - *DMA*
- Memory
  - *Built in RAM / Flash*
  - *External memory*
- Size
- Power consumption



ANALOG DEVICES

SHARC Processor

Preliminary Technical Data

ADSP-21483/21486/21487/21488/21489

SUMMARY

STM32F405xx
STM32F407xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

Features

- Core: ARM 32-bit Cortex™-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 1 Mbyte of Flash memory
  - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
  - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.8 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
  - Up to 3 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs (42 Mbit/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

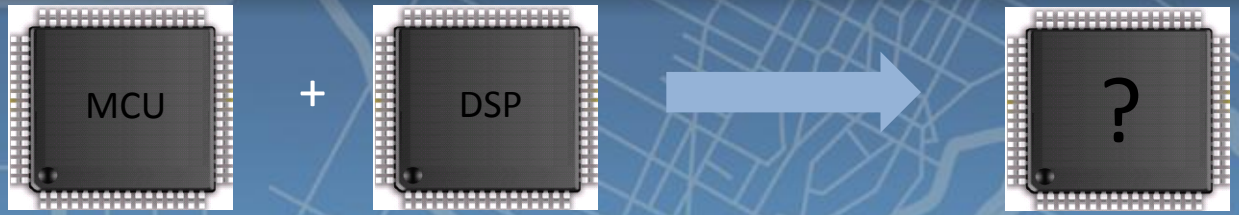
Table 1. Device summary

Reference	Part number
STM32F405xx	STM32F405RG, STM32F405VG, STM32F405ZG, STM32F405OG, STM32F405OE
STM32F407xx	STM32F407VG, STM32F407IG, STM32F407ZG, STM32F407VE, STM32F407ZE, STM32F407IE

June 2013 DocID022152 Rev 4 1/185

This is information on a product in full production. www.st.com

Use 2 Processors?



Connected products require an MCU

- *USB*
- *Wi-Fi / Ethernet*
- *Etc.*

Signal processing needs for multimedia products are growing

- *Audio, video, microphones, etc.*

IoT products packed with sensors

Can a single chip handle all functions?

The ABC's of Processor Choice

Awareness – *I didn't know I could use this processor for audio*

Benchmarking – *Will my application fit?*

Cost – *What is the overall system cost?*

How We'll Compare Architectures

Define a true DSP

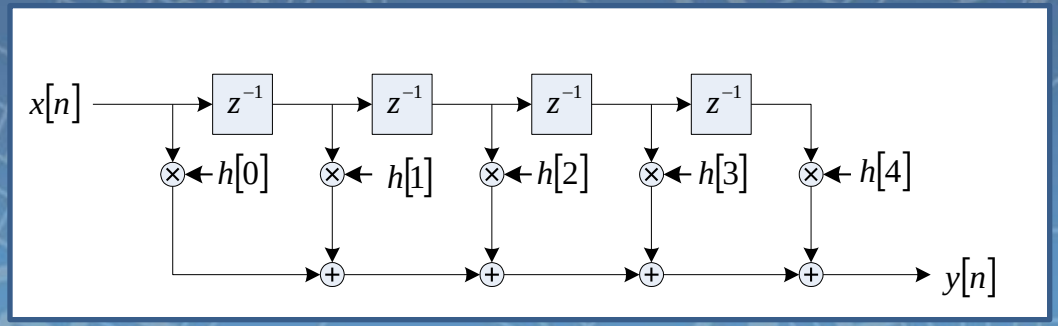
Then consider various processor families

- *ADI SHARC*
- *ADI Blackfin BF53x / BF70x*
- *ARM Cortex-M4 / M7*
- *ARM Cortex-A8/9/15*

A True DSP

- Single cycle multiply - accumulate
- Load and stores in parallel with computation
- Zero-overhead loops
- Circular and bit-reversed addressing

- Accumulator with guard bits
- Fractional and saturating math

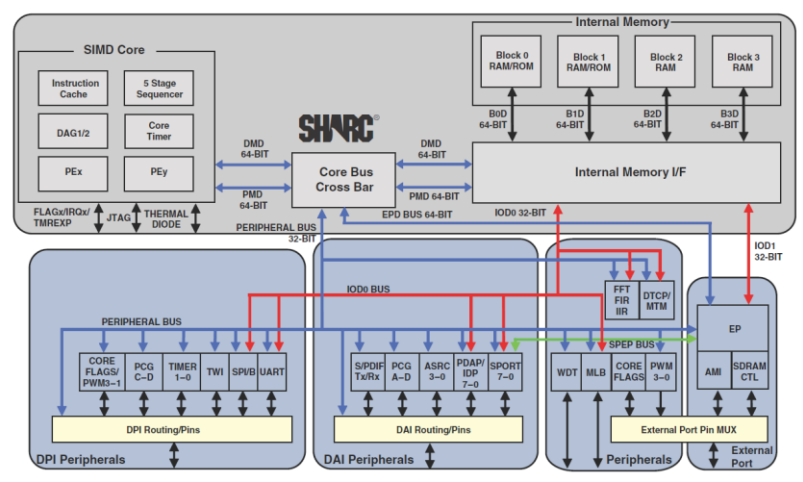


The Test: Can you do an FIR filter in roughly 1 cycle/tap?

SHARC Core

- A True DSP
- Floating-point support
- 2-way SIMD
- Large 5 Mbit internal memory
- No cache

- Hardware accelerators for FIR, IIR, and FFT
- 4 stereo sample rate converters
- S/PDIF transceiver
- Lots of I2S and TDM I/O
- External SDRAM interface

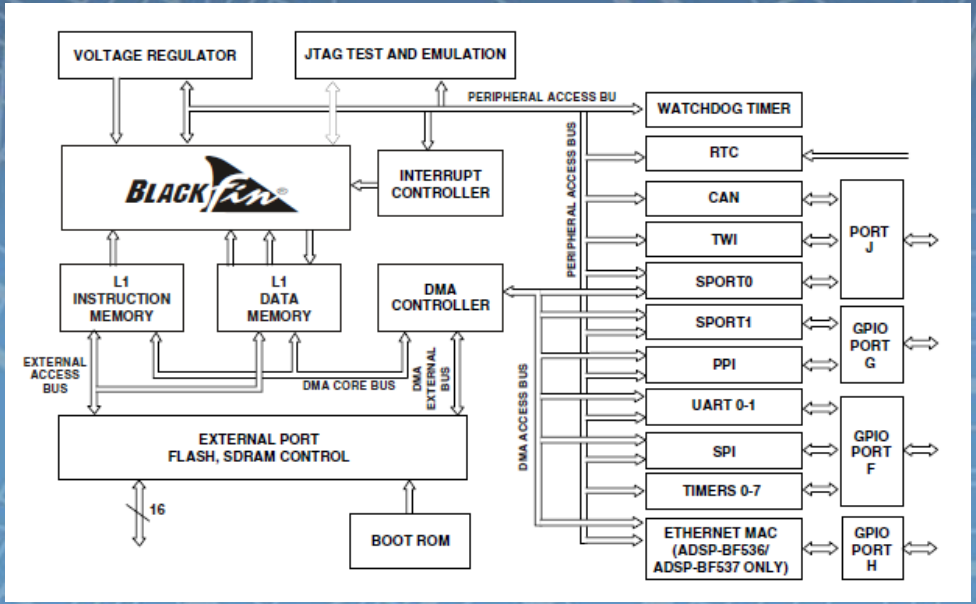


Starting at $8.00

AUDIO AES 137TH AES CONVENTION

Blackfin BF5xx Core

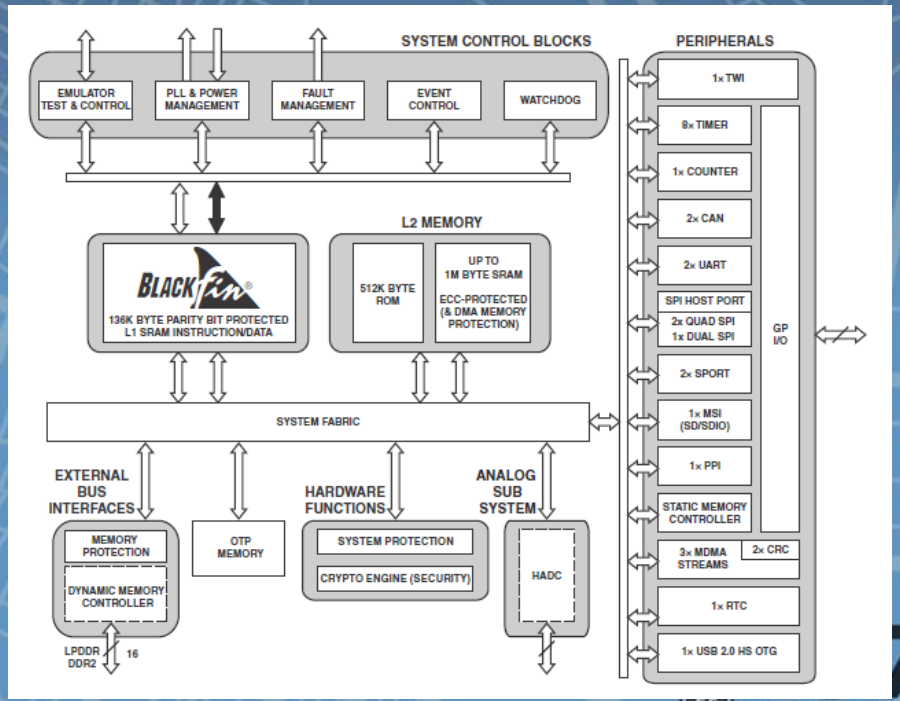
- True DSP
- 32-bit internal registers
- Dual 16-bit MAC
- Data and program cache
- Up to 148 kbytes internal RAM
- USB and Ethernet support



Starting at $2.00

Blackfin BF7xx Core

- True DSP
- 32-bit internal registers
- Dual 32-bit MAC
- Single 16-bit MAC
- Data and program cache
- 136 kbytes internal RAM
- USB support



Starting at $4.00

ARM Cortex-M Series

The Underlying Core

Cortex-M3 released 2004

- *Traditional microcontroller*
- *32-bit native data type. Fixed-point*

Cortex-M4 released in 2010

- *Digital signal controller*
- *Adds floating-point and some DSP capabilities*

Cortex-M7 announced Sept. 2014

- *Further architecture improvements for DSP*

Many Licensees

ST Microelectronics, Freescale, NXP, Atmel, Texas Instruments, Analog Devices, Infineon, etc.

Other Highlights

Basic audio I/O (I2S)

Low power variants

USB and Ethernet

M4 Starting at $1.50

Cortex-M Core Features

	Cortex-M3	Cortex-M4	Cortex-M7	True DSP
Single cycle MAC		Fixed-point only	Fixed and floating-point	Y
Floating-point		Y	Y	Y
Fractional and saturating math		Y	Y	Y
SIMD operations		Y	Y	Y
Load and store in parallel with math			Y (1)	Y (2)
Zero overhead loops			Y	Y
Accumulator with guard bits				Y
Circular and bit-reversed addressing				Y

ARM Cortex-A Processors

Processing engines for a wide variety of consumer products.

"System on Chip" combining processing, I/O, and graphics.

Excellent connectivity

Power efficient

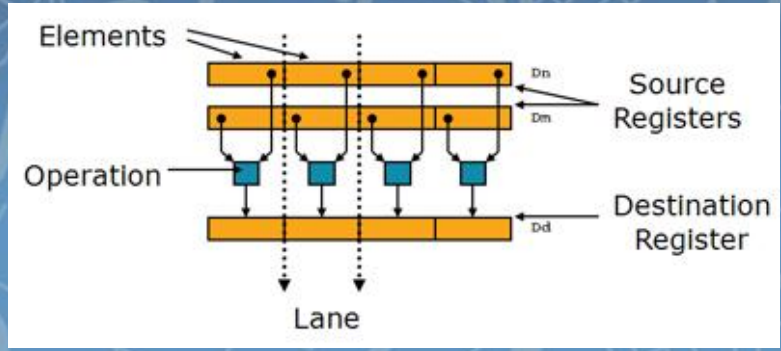
Strong price pressure and devices available from a variety of vendors

Getting better at audio processing

Starting at $5.00

ARM Cortex-A Architecture

- Multicore designs up to 2.5 GHz
  - *1→2→4 processors*
- Family of processors
  - *A5, A7, A8, A9, A15, etc.*
- NEON Technology
  - *SIMD multimedia extensions including 4 way floating-point*
  - *16 x 128-bit registers*
  - *Provides a significant computational boost to audio applications*
- Versions with audio specific peripherals starting to appear



A8/A9/A15 Differences

Cortex-A8

Single core up to 1 GHz

13 stage pipeline

Cortex-A9

Multicore up to 2 GHz

Out of order execution

8 to 11 stage pipeline

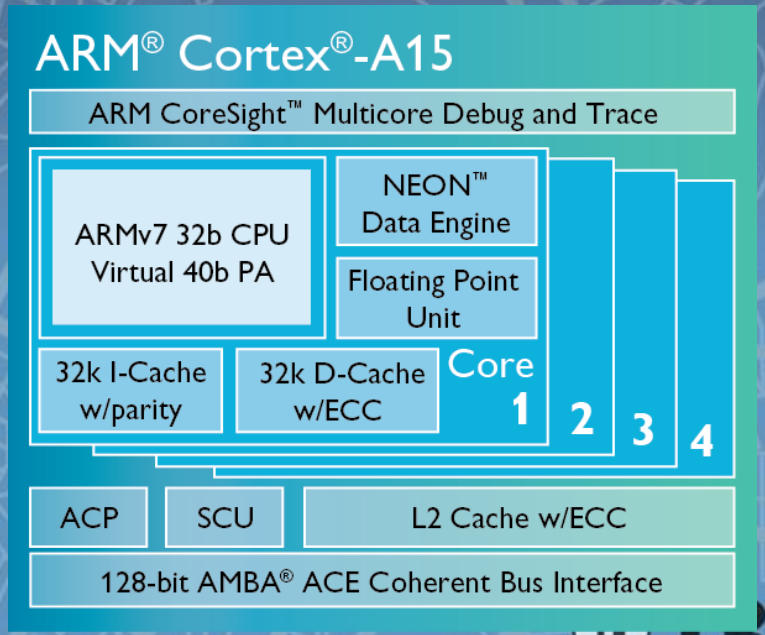
Cortex-A15

Multicore up to 2.5 GHz

Highly out of order execution

17 to 25 stage pipeline

Twice the memory bandwidth from core to cache



Introducing Benchmarks

FIR Filter

Equalizers, adaptive filters

Room correction

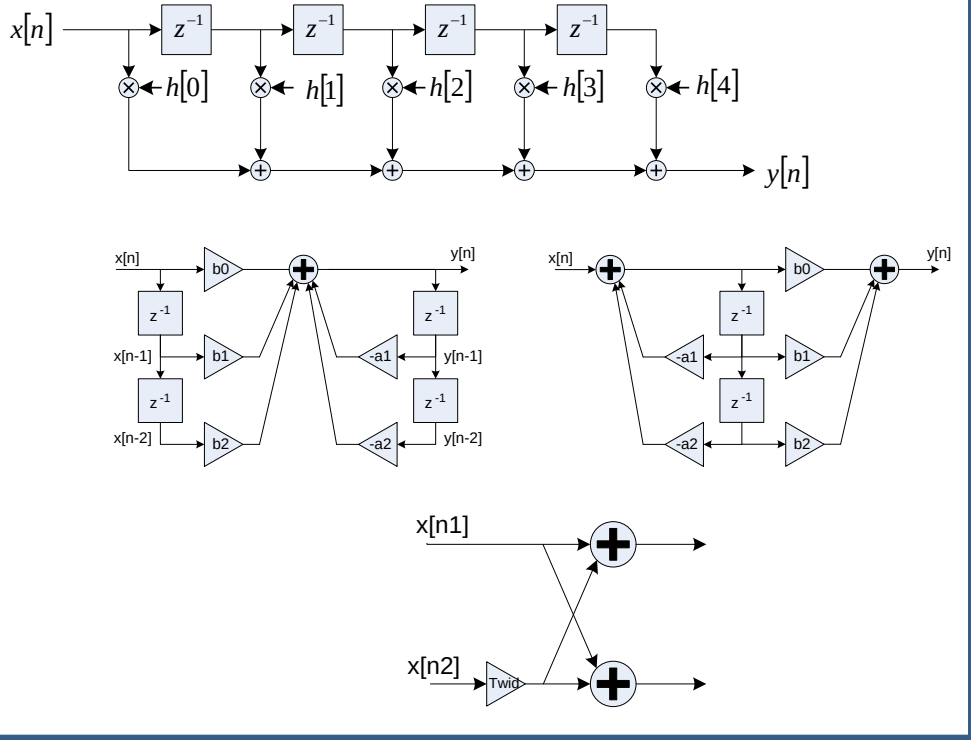
Biquad filter

Audio EQ work horse

PID loops and motor control

FFT

Frequency domain processing



Understanding Benchmarks

Considerations

Memory accesses

MACs

Specialized addressing modes used?

Analysis

N-point FIR – Memory intensive

- *2N+3 memory accesses*
- *N MACs*

Biquad Filter Stage – MAC intensive

- *2 memory accesses*
- *5 MACs*

FFT Butterfly – Balanced

- *10 memory accesses*
- *10 math operations (+ or x)*

SHARC Optimization

Write in ASM code

Utilize SIMD whenever possible

Benchmarks using internal DSP Concepts libraries

```
lcntr=r1, do _sampleLoopEnd until lce;
   f15=f0*f11,r8=dm(i4,m4);
   f8=f3*f5,f15=f8+f15,pm(i12,m12)=r12;
   f10=f0*f6,f2=f8+f15,r0=r3;
   f8=f2*f7,f15=f10+f14,r3=r2;

_sampleLoopEnd:
   f14=f3*f4,f12=f8+f15;
```

Blackfin Optimization

- Write in ASM code
- Utilize SIMD whenever possible
- Internal DSP Concepts libraries and published ADI libraries

```
biquad_filter_start:
        a0 += r3.h * r4.h, a1 += r3.h * r4.l(m)|| r5 = [fp - 12] || NOP;
        a1 += r4.h * r3.l (m) || r6 = [i3++m3] || NOP;
        a0 += r5.h * r6.h, a1 += r5.h * r6.l(m)|| r3 = [fp - 16] || NOP;
        a1 += r6.h * r5.l (m) || r4 = [i3++m3] || r7 = [p3 + 0];
        a0 += r3.h * r4.h, a1 += r3.h * r4.l(m)|| r5 = [fp - 20] ;
        a1 += r4.h * r3.l (m) || r6 = [i3++m3] || [p3 + 4] = r7;
        a0 += r5.h * r6.h, a1 += r5.h * r6.l(m)|| NOP || [p3 + 0] = r0;
        a1 += r6.h * r5.l (m) || r4 = [fp - 4] || r0 = [i0 ++ m0];

        a1 = a1 >>> 15 || r7 = [p3 + 8];
         a0 += a1 || [p3 + 12] = r7;

// And more
```

Cortex-M4 / M7 Optimization

- Write in C code
- Loop unrolled
- Heavy register reuse to minimize data accesses
- Different code for M4 and M7
- Part of the CMSIS DSP library provided by ARM

```
while(sample > 0u) {

      /* y[n] = b0 * x[n] + d1 */
      /* d1 = b1 * x[n] + a1 * y[n] + d2 */
      /* d2 = b2 * x[n] + a2 * y[n] */

      /* Read the first 2 inputs. 2 cycles */
      Xn1  = pIn[0 ];
      Xn2  = pIn[1 ];

      /* Sample 1. 5 cycles */
      Xn3  = pIn[2 ];
      acc1 = b0 * Xn1 + d1;

      Xn4  = pIn[3 ];
      d1 = b1 * Xn1 + d2;

      Xn5  = pIn[4 ];
      d2 = b2 * Xn1;

// and on and on
```

Cortex-A Optimization

- Write in C code with intrinsics
- Loop unrolled
- Heavy register reuse to minimize data accesses
- Same code (mostly) used for all Cortex-A processors
- Internal DSP Concepts libraries

```
while (blockSize >= 16)
 {
    w6 = vld1_dup_f32(src);
    src += srcInc;
    y6 = vmul_f32(b0, w6);
    w1 = vmla_f32(w1, a1, w0);
    w2 = vmla_f32(w2, a2, w0);
    y1 = vmla_f32(y1, c1, w0);
    y2 = vmla_f32(y2, c2, w0);
    vst1_lane_f32(dst, y0, 0);
    dst += dstInc;

    w7 = vld1_dup_f32(src);
    src += srcInc;
    y7 = vmul_f32(b0, w7);
    w2 = vmla_f32(w2, a1, w1);
    w3 = vmla_f32(w3, a2, w1);
    y2 = vmla_f32(y2, c1, w1);
    y3 = vmla_f32(y3, c2, w1);
    vst1_lane_f32(dst, y1, 0);
    dst += dstInc;

// and on and on
```

Ease of Optimization

Cortex-M > SHARC > Cortex-A > BF70x > BF5xx

(easiest) **(hardest)**

FIR Benchmarks

256 sample block size
Clock cycles are shown
Floating-point for all except Blackfin (Q31)
Measured using Audio Weaver

Num Taps	Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin 5xx	Blackfin 70x	SHARC 21489
5	6743	6467	6315	2673			1954
10	9871	9793	9245	5142			2473
20	15650	13598	14338	5031			3777
50	35801	29310	32799	10267	27404	14456	7677
100	67833	53913	62145	15525			14210

FIR Analysis

Cycles per sample per tap

Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin 5xx	Blackfin 70x	SHARC 21489
2.65	2.11	2.43	0.61	2.14	1.13	0.56

Biquad Benchmarks

Num Stages	Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin BF5xx	Blackfin BF70x	SHARC 21489
1	4480	4867	4326	2439	4650	3338	1455
4	16700	16712	17750	9040			5405
8	32900	33354	32933	17825			10650
12	49100	49274	50243	26664			15958

256 sample block size
Clock cycles are shown
Measured using Audio Weaver
Mono channel processing

Blackfin notes
Uses 32x32+64 math
Additional overhead for shifting of data

Biquad Analysis

Cycles per sample per stage

Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin BF5xx	Blackfin BF70x	SHARC 21489
15.98	16.04	16.36	8.68	18.16	13.04	5.19

Faster Biquads

SHARC has 2-way SIMD and can process 2 channels in parallel

NEON has 4-way SIMD and can process 4 channels in parallel (but we don't have this function)

For NEON, we have a "Biquad Cascade Delay" function which implements a cascade by mono Biquad filters with a delay between stages. This allows NEON parallelization

Cycles per sample per stage

Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	SHARC 21489
15.98	14.36	9.49	6.01	2.64

FFT Benchmarks

Length	Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin BF5xx	Blackfin BF70x	SHARC 21489
64	3709	3773	3358	2264	2200	1526	783
128	9811	6384	5682	3830	5249	3431	1334
256	21575	11114	9891	6668	11744	7611	2542
512	37813	21852	19448	13111	27385	17084	5189
1024	96630	50738	45157	30443	60216	37568	10972

Complex transform
No bit reversal

FFT Analysis

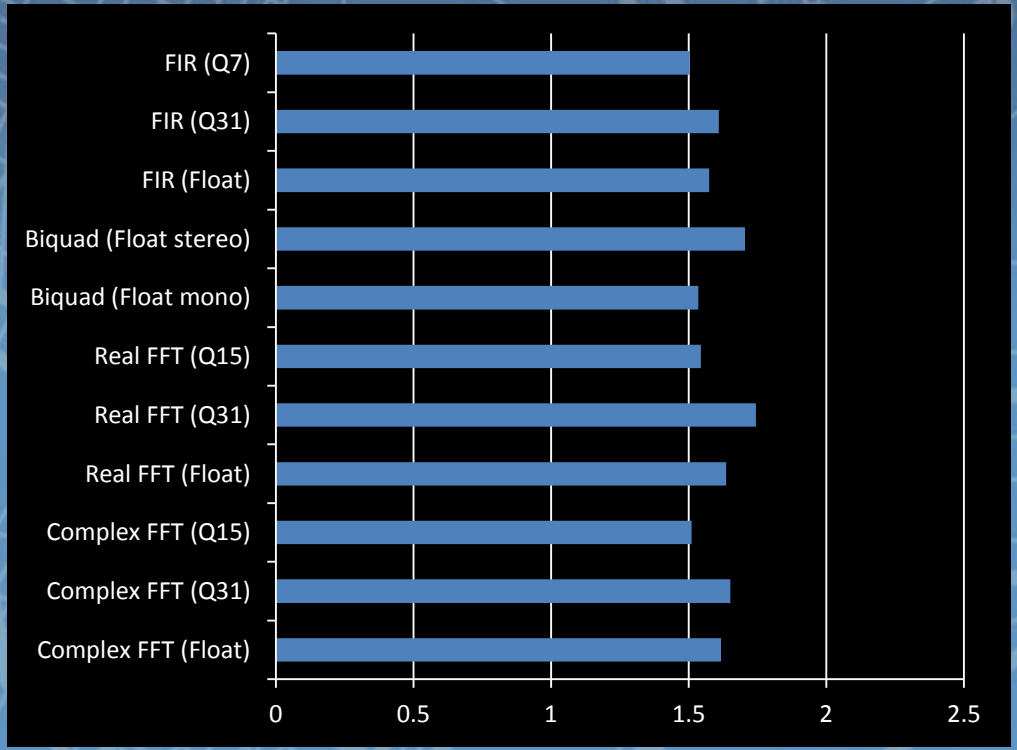
FFT cycle count is proportional to K * N * log2(N)
K factor shown below
Smaller is better

Cortex-M4	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin BF5xx	Blackfin BF70x	SHARC 21489
9.44	4.95	4.41	2.97	5.88	3.67	1.07

Introducing the Cortex-M7

- Announced by ARM on 9/24/14
- Main new feature is improved DSP performance
- Achieved through
  - *Superscalar architecture*
  - *Faster MAC*
  - *Better memory bandwidth*
  - *Clock speed increase to 400 MHz*
- Can only share preliminary information

Chart shows per cycle speed improvements for the M7 vs the M4



Normalized Per Cycle Benchmarks

	Cortex-M4	Cortex-M7	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin 5xx	Blackfin 70x	SHARC 21489
FIR	0.21	0.33	0.26	0.23	0.92	0.26	0.49	1.00
Biquad	0.16	0.28	0.18	0.28	0.44	0.15	0.20	1.00
FFT	0.11	0.17	0.22	0.24	0.36	0.18	0.29	1.00

Performance normalized relative to SHARC
Higher numbers are better

With Processor Speed Differences

	Cortex-M4	Cortex-M7	Cortex-A8	Cortex-A9	Cortex-A15	Blackfin 5xx	Blackfin 70x	SHARC 21489
FIR	0.09	0.29	0.59	0.51	3.05	0.40	0.44	1.00
Biquad	0.07	0.25	0.41	0.62	1.46	0.23	0.18	1.00
FFT	0.05	0.15	0.48	0.54	1.20	0.28	0.26	1.00

Takes into account maximum clock speeds

- Cortex-M4: 204 MHz
- Cortex-M7: 400 MHz
- Cortex-A8: 1 GHz
- Cortex-A9: 1 GHz
- Cortex-A15: 1.5 GHz
- Blackfin 53x: 700 MHz
- Blackfin BF70x: 400 MHz
- SHARC: 450 MHz

Bigger is better

Other Considerations

Complicating Factors

Non-deterministic / data dependent behavior

Long pipelines & processor stalls

Multiple threads

External memory and caches

Operating systems

Fixed vs floating-point

My Rules of Thumb

SHARC bare metal (no OS) - up to 95%

Cortex-M4 bare metal (no OS) – up to 90%

Blackfin bare metal (no OS) – up to 85%

ARM Cortex-A8/9/15 with cache and Linux – up to 65%

Benchmarking Real World Systems with Audio Weaver

AUDIO AES 137TH AES CONVENTION

Audio Weaver- Proprietary Design Tools

Complete audio processing solution

Large library of optimized modules

Graphical editor

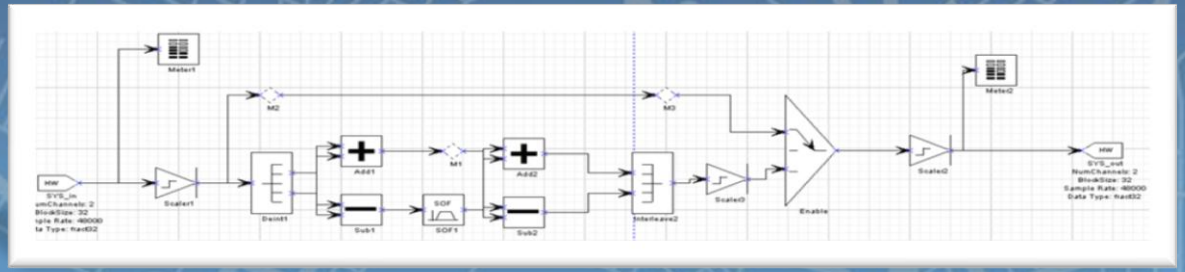
Real-time tuning

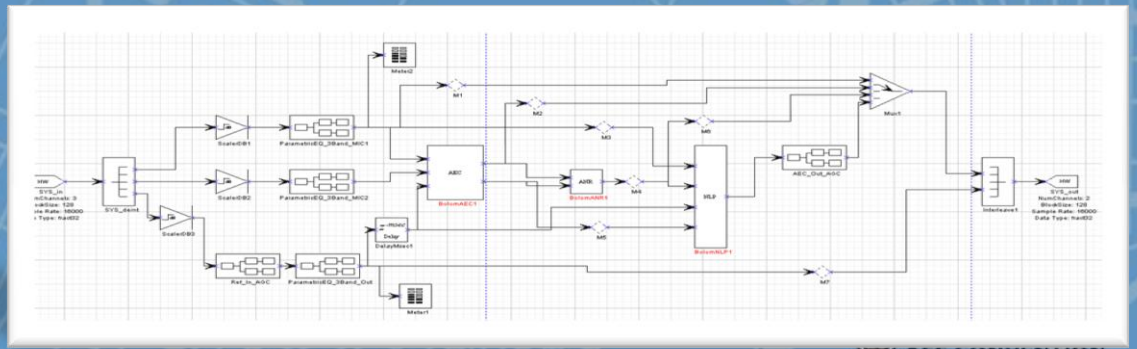
Regression testing

Multirate processing

MIPs and memory profiling

Advanced features using MATLAB





Supports

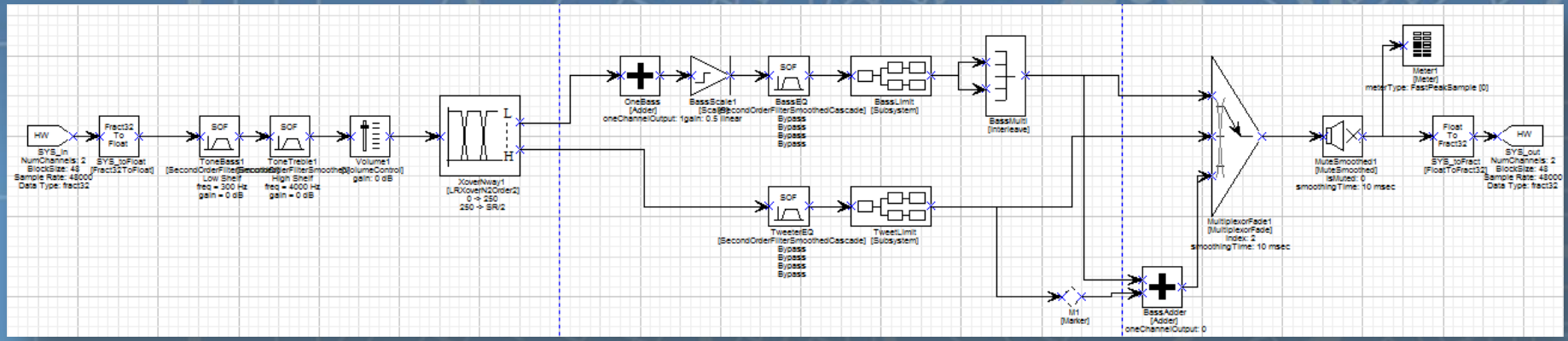
ARM Cortex-M4 / M7

ARM Cortex-A8 /A9 / A15

ADI SHARC and Blackfin

TI C67x

Example: Loudspeaker Processing



Loudspeaker Profile

Module Name	Module Type	M4 MIPS	SHARC MIPS
SYS_toFloat	Fract32ToFloat	0.84	0.28
ToneBass1	SecondOrderFilterSmoothed	2.16	0.63
ToneTreble1	SecondOrderFilterSmoothed	2.13	0.63
Volume1	VolumeControl	2.14	0.73
XoverNway1	LRXoverN2Order2	11.6	3
OneBass	Adder	1.51	0.78
BassScale1	Scaler	0.44	0.25
BassEQ	SecondOrderFilterSmoothedCascade	4.11	2.48
BassLimit	Subsystem	10.14	7.18
BassMulti	Interleave	0.72	0.57
TweeterEQ	SecondOrderFilterSmoothedCascade	8.28	2.57
TweetLimit	Subsystem	11.96	8.16
BassAdder	Adder	0.8	0.39
MultiplexorFade1	MultiplexorFade	0.65	0.46
MuteSmoothed1	MuteSmoothed	1.49	0.36
SYS_toFract	FloatToFract32	2.17	0.37
Meter1	Meter	2.03	1.02
Totals		63.16	29.86

Cortex-M7 results not available but we estimate M7 CPU load as 40 to 42 MHz.

Example High-End Automotive System

12 Channel High End System

Stereo entertainment content

8 announcement channels

Spectrum analyzer

Graphic equalizer

Speed dependent equalizer

Perceptual volume control

2 to 7.1 channel upmix

Announcement channel duckers

> 100 Biquads for speaker equalization

Separate compressor/limiter per channel

Time delays

Test signal generation for factory tests

443 individual audio modules from 57 different module classes

Automotive Profile

SHARC (21489. 400 MHz)

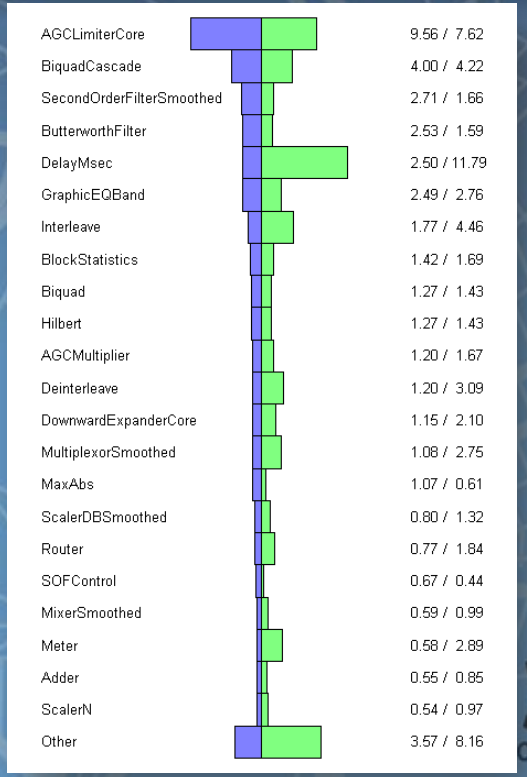
265 MHz = 66.3%

Cortex-A9 (TI OMAP 4430. 1 GHz)

914 MHz = 92%

Cortex-A15 (TI OMAP 5432. 1.5 GHz)

649 MIPs = 43%



Audio Weaver Business Model

Pricing

Free for prototyping, evaluation, and benchmarking

Utilize one of our supported evaluation boards

Pay to obtain processor specific libraries ($1k/per processor family)

Pay unit royalties when you ship products

Eval Boards

EZ-KITs from ADI (SHARC & BF)

SHARC audio hardware from Danville Signal

STM32F407 Discovery board (M4)

Multiple Linux-based eval boards for Cortex-A (Panda, BeagleBone, etc)

Increasing the Pace of Innovation

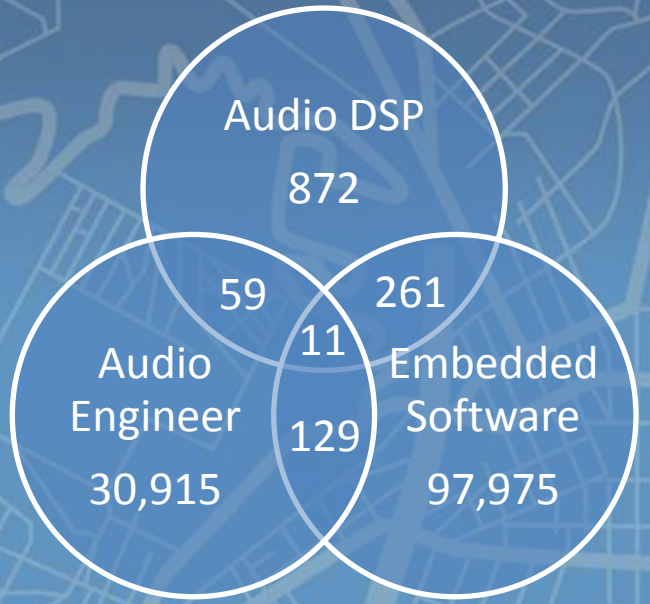
By creating an ecosystem for audio product development

Chris Anderson – ARM TechCon Keynote on 10/3/14

From difficult to easy

From expensive to cheap

From closed to open



Conclusion

There are many more choices now for audio processors

Benchmarks are useful but only take you so far

To minimize risk you need to prototype your processing and run on the actual device

Thank You!

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